OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

AUTUMN EXAMINATIONS 2009

BSc Honours

Computer Science

CS4403 Introduction to Embedded Systems

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Professor James Bowen
Dr. Richard Studdert

Answer all questions
(Total 80 Marks)

Time 11/2 Hours

Q1. Figures 1 and 2 shows how the address signals appearing on lines AD_0 - AD_7 are latched and buffered using an SN74LS374 IC.
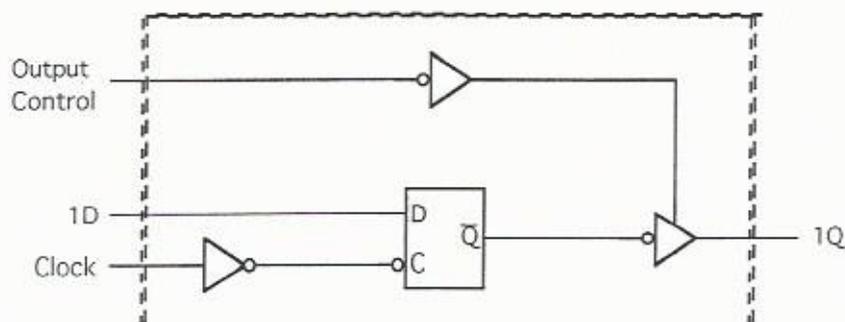

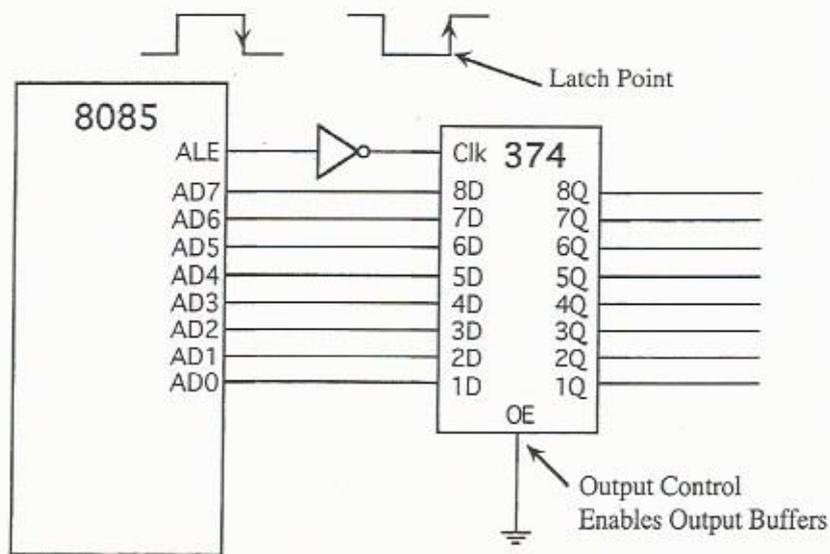Figure 1

Figure 2

(a) Explain the operation(s) portrayed by Figures 1 and 2.   *10 Marks*

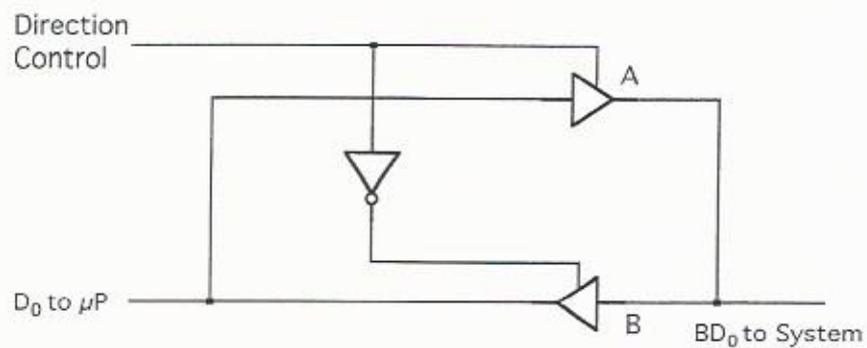(b) Explain how the circuit in Figure 3 can be used to buffer a data line.   *6Marks*

Figure 3

Q2. Handshake Input

In Figure 4 an 8-bit input device is configured for Handshake I/P at port 1. The STATUS flag is connected to bit 7 of I/P port 0. Explain, with reference to Figure 4 and the program code, the sequence of operations corresponding to reading the data.
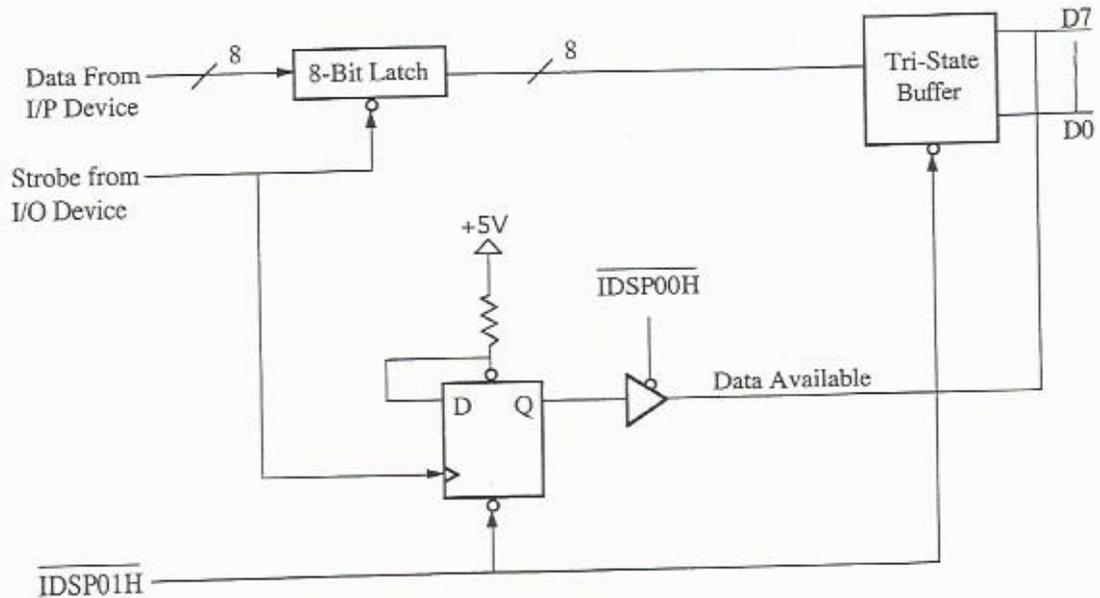

Figure 4

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INP:  IN 00H
      ANI 80H
      JZ INP
      IN 01H
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Q3(a)   Describe the 2-D address organisation used in static MOS IC memory design. Illustrate your answer using a 256 Kbit ROM memory IC organised as 32Kx8. In particular, show how the logical word is extracted from the physical word.   *(12 Marks)*

(b)   What differences in organization would be necessary if the IC in (a) were RW.   *(2 Marks)*

(c)   What differences from the IC in (b) would be necessary if the RW IC was organized as 256 Kbit x 1.   *(2 Marks)*

Q4. Interrupt Input

Figure 5 shows how a device can be connected to a vector interrupt on the 8085 processor using a Restart instruction. Explain how it works.

The RESTART instruction

$$RST\ n \qquad 0 \le n \le 7$$

consists of the following micro-operations:

((SP) - 1) ¬ (PCH)   Load contents of PC onto the stack
((SP) - 2) ¬ (PCL)
(SP)   ¬ (SP) - 2   Decrement stack pointer

(PC)   ¬ 8*n   Place the restart address, i.e. 8*n, in the PC
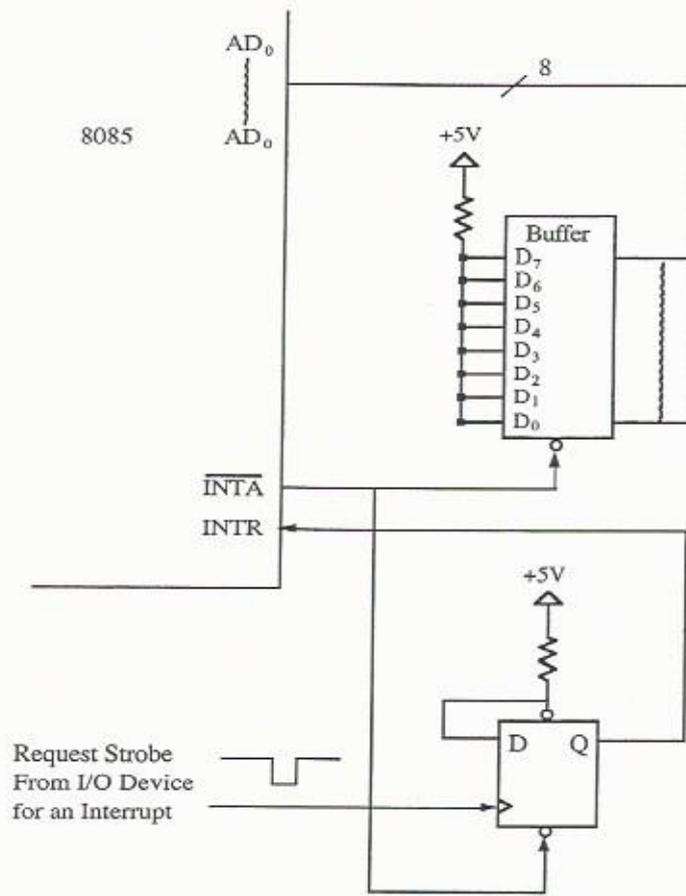

Figure 5

Q5. Serial Transmission

(a)   In the context of asynchronous serial transmission:

    (i)   In what way is it asynchronous and at what level is it synchronous?   2 Marks

    (ii)   What functions do the start and stop bits perform and what should be their polarities?   2 Marks

    (iii)   Why should the receiver clock rate be a multiple of the bit rate?   2 Marks

    (iv)   What is meant by "echo checking" and how and why is it used?   2 Marks

(b) In the context of synchronous serial transmission:

    (i)   In what circumstances are character oriented and bit oriented protocols used?   2 Marks

    (ii)   What levels of synchronisation are used in bit oriented transmission?   2 Marks

    (v)   How (and why?) is data transparency effected in bit oriented transmission?   4 Marks